Amendments

In the Claims:

Please cancel claims 41-46, 48-52, 54-66, 68-71 and 73-78 without prejudice or disclaimer.

Please substitute the following claims 47 and 67 for the pending claims 47 and 67:

47. (Once Amended) A computer-based method for providing extended precision in single instruction multiple data (SIMD) arithmetic operations, comprising the steps of:

(a) loading a first vector into a first register, said first vector comprising a plurality of N-bit elements;

(b) loading a second vector into a second register, said second vector comprising a plurality of N-bit elements;

(c) executing an arithmetic instruction for at least one pair consisting of an N-bit element in said first register and an N-bit element in said second register, to produce a resulting element;

(d) writing said resulting element into an M-bit element of an accumulator, wherein M is greater than N;

(e) transforming said resulting element in said accumulator into a width of N-bits; and

(f) writing said resulting element into a third register;

wherein said accumulator comprises a plurality of M-bit elements and wherein steps (c)-(f) operate on a plurality of elements of said first and second vectors to produce a resultant vector formed from a plurality of resulting elements written to said third register; and

wherein said resulting elements in said accumulator are wrapped around the representable range of said resulting elements.

4 ~~53.~~ (Once Amended) The method as recited in claim ~~80~~ 3, wherein said rounding step comprises one of:

rounding said resulting element towards zero;

rounding said resulting element towards the nearest unit, wherein said resulting element is rounded away from zero if said resulting element is at least halfway towards the nearest unit; and

rounding said resulting element towards the nearest unit, wherein said resulting element is rounded towards zero if said resulting element is at least halfway towards the nearest unit.

~~67.~~ 8 (Once Amended) A processor for providing extended precision in single instruction multiple data (SIMD) arithmetic operations, comprising:

means for executing an arithmetic instruction involving an element of a first vector and an element of a second vector to produce a resulting element, said first and second vector comprising a plurality of N-bit elements;

an accumulator for receiving said resulting element, wherein said resulting element is stored in an M-bit element of said accumulator and wherein M is greater than N;

means for transforming said resulting element in said accumulator into a width of N-bits; and

means for writing said transformed resulting element to a register;

wherein said accumulator comprises a plurality of M-bit elements and wherein said means for executing is repeated for said plurality of elements of said first and second vectors to produce a plurality of resulting elements that are received by said accumulator and wherein said means for transforming and said means for writing are performed on said plurality of resulting elements; and

wherein said resulting elements in said accumulator are wrapped around the representable range of said resulting elements.

~~72.~~ 6 The processor as recited in claim ~~82~~ 5, wherein said rounding means comprises one of:

means for rounding said resulting element towards zero;

means for rounding said resulting element towards the nearest unit, wherein said resulting element is rounded away from zero if said resulting element is at least halfway towards the nearest unit; and

means for rounding said resulting element towards the nearest unit, wherein said resulting element is rounded towards zero if said resulting element is at least halfway towards the nearest unit.

Please add the following new claims 79-82:

79. A computer-based method for providing extended precision in single instruction multiple data (SIMD) arithmetic operations, comprising the steps of:

(a) loading a first vector into a first register, said first vector comprising a plurality of N-bit elements;

(b) loading a second vector into a second register, said second vector comprising a plurality of N-bit elements;

(c) executing an arithmetic instruction for at least one pair consisting of an N-bit element in said first register and an N-bit element in said second register, to produce a resulting element;

(d) writing said resulting element into an M-bit element of an accumulator, wherein M is greater than N;

(e) transforming said resulting element in said accumulator into a width of N-bits;

(f) dividing said resulting elements stored in said accumulator into a plurality of subsets;

(g) writing each subset to at least one of a plurality of registers, each of said plurality of registers having a width smaller than said accumulator width; and

(h) writing said resulting element into a third register;

wherein said accumulator comprises a plurality of M-bit elements and wherein steps (c)-(h) operate on a plurality of elements of said first and second vectors to produce a resultant vector formed from a plurality of resulting elements written to said third register.

80. A computer-based method for providing extended precision in single instruction multiple data (SIMD) arithmetic operations, comprising the steps of:

(a) loading a first vector into a first register, said first vector comprising a plurality of N-bit elements;

(b) loading a second vector into a second register, said second vector comprising a plurality of N-bit elements;

(c) executing an arithmetic instruction for at least one pair consisting of an N-bit element in said first register and an N-bit element in said second register, to produce a resulting element;

(d) writing said resulting element into an M-bit element of an accumulator, wherein M is greater than N;

(e) transforming said resulting element in said accumulator into a width of N-bits, wherein said transforming comprises shifting said resulting element in said accumulator for scaling the value of said resulting element, rounding said resulting element and clamping said resulting element; and

(f) writing said resulting element into a third register.

81. A processor for providing extended precision in single instruction multiple data (SIMD) arithmetic operations, comprising:

means for executing an arithmetic instruction involving a first plurality of elements of a first vector and a second plurality of elements of a second vector to produce a plurality of resulting elements, said first and second vector comprising a plurality of N-bit elements;

an accumulator for receiving said plurality of resulting elements, wherein said plurality of resulting elements are each stored in one of a plurality of M-bit elements of said accumulator and wherein M is greater than N;

means for transforming said plurality of resulting elements in said accumulator into a width of N-bits;

means for dividing said plurality of resulting elements stored in said accumulator into a plurality of subsets; and

means for writing each subset to at least one of a plurality of registers, each of said plurality of registers having a width smaller than said accumulator width.

5

~~82.~~ A processor for providing extended precision in single instruction multiple data (SIMD) arithmetic operations, comprising:

means for executing an arithmetic instruction involving an element of a first vector and an element of a second vector to produce a resulting element, said first and second vector comprising a plurality of N-bit elements;

an accumulator for receiving said resulting element, wherein said resulting element is stored in an M-bit element of said accumulator and wherein M is greater than N;

means for transforming said resulting element in said accumulator into a width of N-bits, wherein said means for transforming comprises means for shifting said resulting element in said accumulator for scaling the value of said resulting element, means for rounding said resulting element, and means for clamping said resulting element; and

means for writing said transformed resulting element to a register.